Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-14. Cancelled

15. (Currently Amended) A memory cell, comprising:

a conducting element at least partially disposed within a substrate;

a bottom electrode at least partially disposed on a surface of the substrate and having a sidewall operatively coupled with the conducting element; and

phase change material at least partially disposed on the surface of the substrate and operatively coupled with the sidewall of the bottom electrode.

16. (Original) The memory cell as set forth in Claim 15, wherein:

the bottom electrode has dimensions of length, height, and width;

the bottom electrode has its length substantially parallel to the substrate;

the bottom electrode includes a plane end surface formed substantially at a right angle to the length; and

the plane end surface forms an operative contact with the phase change material.

17. (Original) The memory cell as set forth in Claim 15, further comprising a pad layer disposed on the surface of the substrate wherein the bottom electrode is formed on a sidewall of the pad layer.

18. (Original) The memory cell as set forth in Claim 17, wherein:

the pad layer comprises a top surface, a bottom surface, and at least two sidewalls disposed between the top and bottom surfaces; and

the bottom electrode is formed on one of the at least two sidewalls.

19. (Currently Amended) The memory cell as set forth in Claim 18, the conducting element comprising a first conducting element, the bottom electrode comprising a first bottom electrode, and the memory cell further comprising:

a second conducting element at least partially disposed within the substrate; and

a second bottom electrode formed on another one of the at least two sidewalls of the pad layer, the second bottom electrode being operatively coupled with the second conducting element, wherein the phase change material is operatively coupled with the second bottom electrode.

20. (Currently Amended) The memory cell as set forth in Claim 19, wherein the first and second conducting elements are formed of one or more of tantalum nitride, titanium nitride, titanium tungstide, titanium, tungsten, doped polysilicon, and combinations thereof.

21. (Original) The memory cell as set forth in Claim 19, wherein the pad layer is disposed between the first bottom electrode and the second bottom electrode.

22. (Original) The memory cell as set forth in Claim 15, further comprising a top electrode disposed on the phase change material.

23. (Original) The memory cell as set forth in Claim 15, wherein the phase change material comprises chalcogenide material.

24. (Currently Amended) An array of memory cells formed at least partially in a substrate, the array being organized into rows and columns with memory cells at intersection of rows and columns, each memory cell in the array comprising a transistor having a source, a drain, and a gate, the gates of transistors in each column being operatively connected with a common word line, and the drains of transistors in each row being operatively connected with a common bit line, each memory cell comprising:

a conducting element at least partially disposed within the substrate, the conducting element being operatively connected with the source of a corresponding transistor;

a pad layer disposed on the substrate;

a bottom electrode formed on a sidewall of the pad layer, the bottom electrode being operatively coupled with the conducting element;

phase change material at least partially disposed on the substrate and operatively coupled with a sidewall of the bottom electrode; and

a top electrode formed of conducting material disposed on the phase change material and establishing operative contact with the phase change material.

25. (Original) The array of memory cells as set forth in Claim 24, wherein the phase change material comprises chalcogenide material.

26. (New) The memory cell as set forth in Claim 15, wherein the bottom electrode is formed of formed of one or more of tantalum nitride, titanium nitride, titanium tungstide, titanium, tungsten, doped polysilicon, and combinations thereof.

27. (New) A memory cell, comprising:

first and second conducting elements at least partially disposed within a substrate;

a pad layer disposed on a surface of the substrate and comprising a top surface, a bottom surface, and at least two sidewalls between the top and bottom surfaces;

first and second bottom electrodes at least partially disposed on the surface of the substrate and formed on two of the at least two sidewalls, the first and second bottom electrodes being operatively coupled with the first and second conducting elements; and

phase change material at least partially disposed on the surface of the substrate and operatively coupled with the first and second bottom electrodes.

28. (New) The memory cell as set forth in Claim 27, wherein the first and second conducting elements are formed of tungsten.

29. (New) The memory cell as set forth in Claim 27, wherein the pad layer is disposed between the first bottom electrode and the second bottom electrode.